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or more amplifiers to a different one of the clock wires of the clock generator" are missing. Applicant respectfully submits that examples of the amplifiers (which are optional – see paragraph 0052) as referenced in claim 6 are shown in at least Figures 3 and 5. The optional amplifiers are purposely omitted from certain other Figures to reduce clutter (e.g., see paragraph 0057 and Figure 4; paragraph 0062 and Figure 7).

The drawings corresponding to claim 11 are objected to on the basis that the following features: "a plurality of sets of synchronous logic each coupled to a different one of the clock wires, wherein the plurality of set of synchronous logic are interconnected" are missing. With regard to the interconnected synchronous logic of claim 11, Applicant respectfully submits that examples of the possibility of interconnected synchronous logic are shown in at least Figures 3, 4, 5 and 7 as described in the specification in at least paragraphs 0044 and 0052. Specifically, Applicant respectfully submits that the possibility of interconnected synchronous logic driven by a distributed clock is generally understood by those skilled in the art and is a "conventional feature", within the meaning as defined in 37 CFR 1.83(a); and is thus represented graphically for example, by the space outside the cells in at least Figures 3, 4, 5 and 7.

Claims 1-4 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Bushman et al. (U.S. Patent No. 6,657,502).

Independent claim 1:

Independent claim 1 includes the element of "a clock generator, distributed over an integrated circuit, including a plurality of cells each coupled to multiple adjacent ones of said plurality of cells by different clock wires, wherein, for each of said plurality of clock wires, the cell on one end generates the rising edge and the cell on the other end generates the falling edge." (Emphasis added).

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Bushman discloses a multiphase quadrature Voltage Controlled Oscillator (VCO), which can be integrated onto a single integrated circuit chip producing at least two output clock signals 90 degrees out of phase with each other.

Bushman describes in Figure 6 a VCO configuration consisting of four cells (e.g., cell 1 = 134' and 134"; cell 2 = 136' and 136"; cell 3 = 138' and 138" etc.), each consisting of a pair of inverter amplifiers, where each inverter amplifier may be implemented as illustrated in Figure 7A, 7B, or 7C. By way of example, the outputs of 134' and 134" are coupled together to form the output of cell 1 and provide the inputs to 136" and 138'. The cell consisting of 134' and 134" generates both the rising and falling edge of the clock on line Q (at node 142), which is the input to both: 1) the cell consisting of 138' and 138"; and 2) the cell 136' and 136". By using Figure 7A as a specific example, the output 156 of both 134' and 134" (collectively forming cell 1) generates the rising and falling edge with V_{dd} and V_{ss}; while the input of both 138' and 136" simply receive that clock. Thus, in contrast to Applicant's claim 1 where "for each of said plurality of clock wires, the cell on one end generates the rising edge and the cell on the other end generates the falling edge", Bushman's VCO in Figure 6 illustrates that a cell on one end of a clock wire generates both the rising and falling edges, but the two cells on the other end of the same wire only receive and cannot generate a rising or falling edge with respect to that clock wire. This is equally true for each cell represented by a pair of inverter amplifiers in any configuration represented in Figures 7A – 7C. In other words, none of the inverter amplifiers can generate either a rising or falling edge on the wire labeled as input in Figures 7A, 7B, and 7C. Therefore, in Bushman's VCO, for each of a plurality of clock wires, only <u>one cell</u> on one end generates <u>both</u> the rising and falling edge.

Furthermore, Bushman does not make obvious claim 1 either. The distinction discussed above is made more apparent in view of Bushman's goal of generating multiple clocks (with different phases). In contrast, an advantage of the limitations of claim 1 is a

clock generator distributed over the integrated circuit with cells that may work together to synchronize the phase of a clock signal.

Dependent Claims 2-4 and 10:

Claims 2-4 and 10 are dependent on claim 1. For at least this reason, they are allowable over Bushman.

Claims 1, 2, 4, 6-12, 14, and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Milshtein et al. (U.S. Patent No. 6,531,897).

Independent claim 1

Regarding claim 1, Milshtein uses a series of self-timed circuits and self-terminating circuits, referred to as cells in the Office Action, to control the initiation and termination of a pre-charge pulse to various domino nodes 139, 153, 155 and 159. The signal to control initiation and termination of the pre-charge pulse originates from a centrally located pulsed clock generator 134. The self-timed circuitry 111-113 and the self-terminating circuitry 106-109 merely function as a means to respectively initiate and terminate the pre-charge pulse at the domino nodes so that the clock signal from the centrally located pulsed clock generator can be propagated throughout the circuit 100.

Furthermore, inspection of the clock wires connecting the cells reveals that each of the cells and the centrally located pulsed clock generator individually generates both the rising and falling edge on the output clock wires extending there from. For example, the connection and circuitry is designed such that a self-initiating circuit generates both a rising and falling edge to the wire connecting to a self-terminating circuit, but this self-terminating circuit cannot generate a rising or falling edge on this same wire connecting to the self-initiating circuit. Overall, the relationship of the cells is that the clock signal activates a self-timed circuit to initiate a pre-charge pulse at each domino node, and

activates a self-terminating circuit to terminate a pre-charge pulse. Thus Milshtein fails to anticipate at least the claim language previously discussed "for each of said plurality of clock wires, the cell on one end generates the rising edge and the cell on the other end generates the falling edge."

This distinction is made more apparent in view of Milshtein's centrally located pulsed clock generator, in comparison to claim 1's "a clock generator, distributed over an integrated circuit, ..."

Independent Claim 11:

Independent claim 11 includes the element of "a clock generator to generate a clock signal through the interaction of a plurality of cells distributed in grid over an integrated circuit, wherein each of said plurality of cells is coupled to multiple adjacent complementary ones of said plurality of cells by different clock wires; and a plurality of sets of synchronous logic each coupled to a different one of the clock wires, wherein said plurality of sets of synchronous logic are interconnected." (Emphasis added).

As previously described, Milshtein discloses the use of one centrally, located pulsed clock generator to generate the clock signal. The plurality of circuits 106-109 and 111-113 are used to distribute the clock signal by initiating and terminating the pre-charge pulses at various domino nodes. These circuits react to the input provided; they do not "interact" to generate the clock signal as required by claim 11.

This distinction is made more apparent in view of Milshtein's centrally located pulsed clock generator, in comparison to claim 1's "a clock generator to generate a clock signal through the interaction of a plurality of cells distributed in grid over an integrated circuit"

Dependent claims 2, 4, 6 – 10, 11, 12, 14, 18 - 20

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Dependent claims 2, 4, 6 -10 depends on independent claim 1 and dependent claims 11, 12, 14, 18-20 depends on independent claim 11. For at least this reason, claims 2, 4, 6 – 10, 11, 12, 14, 18 – 20 are patentable over Milshtein.

Claims 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Milshtein et al. in view of Graef (U.S. Patent No. 6,305,001).

Claim 13 is dependent upon independent claim 11. For at least this reason, claim 13 is patentable over Milshtein in view of Graef.

Claims 11-14, 16, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bushman et al. in view of Potter et al. (U.S. Patent No. 6,118,304).

Independent Claim 11

As described above, Bushman discloses a multiphase quadrature VCO producing at least two output clock signals 90 degrees out of phase with each other. Applicant's claim 11 requires "a clock generator to generate a clock signal through the interaction of a plurality of cells distributed in grid over an integrated circuit, wherein each of said plurality of cells is coupled to multiple adjacent complementary ones of said plurality of cells by different clock wires; ..." As illustrated in Figure 6 of Bushman, each cell comprises a pair of structurally identical inverting amplifiers where each inverter amplifier consists of one of the configurations illustrated in Figures 7A – 7C and is the same; thus, the cells of Bushman do not satisfy the meaning of complementary.

Potter discloses a "master global clock distributed in a low-skew manner over a relevant clock domain area coupled with a plurality of clocks generated locally by buffering and delaying the rising or falling edge of the master clock" (Col. 10, Lines 59 – 63). Potter has a master clock signal propagating over a distributive network much like Milshtein instead of "a clock generator to generate a clock signal through the interaction

of a plurality of cells ... each of said plurality of cells is coupled to multiple adjacent complementary ones of said plurality of cells by different clock wires..." as required by claim 11. Thus, Potter fails to cure the deficiency of Bushman.

This distinction is made more apparent in view of Bushman's goal of generating multiple clocks with different phases and Potter's goal of having "a plurality of clock signals each with an approximately 50% duty cycle and overlapping phases" (Col 10 lines 33-35). In contrast, the limitation of claim 11 requries "a clock generator with cells distributed in grid over an integrated circuit ..." that interact; which allows for synchronization of the pulse of a clock signal.

Dependent claims 14, 16, 18 and 19

Dependent claims 14, 16, 18, and 19 are dependent upon independent Claim 11. At least for this reason, they are patentable over Bushman in view of Potter.

Intended Use

Under the 35 U.S.C. 102 Claim Rejections, in regard to claims 8 and 9, the Office Action states that "... the intended use of the shape of the apparatus is likewise met." (Office Action, p. 4) (Emphasis added) Under the 35 U.S.C. 103 Claim Rejections, in regard to claim 11, the Office Action states that "The apparatus of Bushman et al. meets all of the claimed limitations of claim 11 except for a plurality of sets of synchronous logic each coupled to a different one of the clock wires, which is considered to be an intended use." (Office Action, p.5) (Emphasis added).

Applicant wishes to clarify the meaning of the language "intended use" cited in the Office Action associated with the claims mentioned above. According to the MPEP §2111.02, issues relating to "intended use" or "purpose" of the invention are often only raised as issues in association with the claim preamble. MPEP §2111.02 states that "intended use" is improperly used if "the body of a claim fully and intrinsically sets forth

all of the limitations of the claimed invention" and that "a patentee defines a structurally complete invention in the claim body."

Applicant respectfully submits that these claims do not use language like a clock generator "for use" with _____, but instead specifically require limitations be present. Specifically, Applicant respectfully submits that there is no intended use of the shapes of the integrated circuits in Claims 8 and 9, but rather, the square, rectangular, and irregular shaped integrated circuits are explicitly required in the body of those claims. Similarly, the body of Claim 11 requires a plurality of sets of synchronous logic each coupled to a different clock wire, and that the plurality of sets of synchronous logic are interconnected.

Therefore, Applicant feels it necessary to clarify the meaning of the statements in the Office Action and request the Examiner to indicate if the meaning is contrary to what is stated above.

Allowable Subject Matter

While Applicant thanks the Examiner for allowing certain claims, Applicant wants to clarify the record with regard to the statements in the Office Action concerning the claims. The Office Action states that claims 5, 15, 17, 21, 30, 39, 52, 62, and 75 have "specific structural limitations such as ..." (Office Action 1/13/2005, pp. 6-8). Further, the Office Action chooses different figure elements for different claims (e.g., cells 401-416 for claim 5 and cells 701-716 for claim 21). Applicant would like to clarify that the Office Action merely uses the elements in the figures as examples and that these examples are not intended and should not be used to read limitations into the claims.

Applicant submits that according to MPEP §2111.01, claims must be given their "broadest reasonable interpretation" while examined by the USPTO and that "the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification"; also "ordinary, simple English words whose meaning is clear and unquestionable, absent any indication that their use in a particular context

changes their meaning, are construed to mean exactly what they say"; and "a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment." The only exception is "when an element is claimed using language falling under the scope of 35 U.S.C. 112, 6th paragraph." However, none of the claims are means plus function claims which would prompt any reference to the specification to clarify the scope of what is claimed.

Here, the plain meaning of the claim language is clear on its face. In addition, the claim language is broader and covers additional embodiments described in the specification than those specifically used as examples in the office action (e.g. at least cells 301-316, 501-528, and 701-716 are also within the scope of claim 5; at least cells 301-316, 401-416 and 501-528 are within the scope of claim 21 etc.) Further, the specification discusses alternatives in at least paragraphs 0059, 0076, 0078 and 0079.[1]

For at least these reasons, Applicant feels it necessary to clarify the meaning of the statements in the Office Action and request the Examiner to indicate if the meaning is contrary to what is stated above.

CONCLUSION

Applicant respectfully submits that the rejections have been overcome by the remarks, and that the Claims are in condition for allowance. Accordingly, Applicant respectfully requests the rejections be withdrawn and the Claims be allowed.

[1] In reference to the example of how the cells can be arranged to accommodate integrated circuits of irregular shapes, paragraph [0059] states that "It should be understood that any shape is within the scope of Furthermore, paragraph [0076] states that "embodiments of the invention has been described in relation to two dimensional fabrication techniques, other embodiment of the invention are implementable using three dimensional fabrication techniques" and that "other topologies are also within the scope of the invention."

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Invitation for a telephone interview

The Examiner is invited to call the undersigned at 408-720-8300 if there remains any issue with allowance of this case.

Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: _____, 2005

_____

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